

CBCS SCHEME

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18EE35

Third Semester B.E. Degree Examination, July/August 2022 Digital System Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Explain the definition of combinational logic. Convert the given Boolean expression into minterm canonical form and maxterm canonical form $F(x, y, z) = X + \overline{XZ}(y + z)$. (08 Marks)
 - Simplify the function : $y = f(a, b, c, d) = \sum m(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$ using Karnaugh map. (06 Marks)
 - Simplify the function : $y = f(a, b, c, d) = \pi M(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$ using the Karnaugh map. (06 Marks)

OR

- Simplify using the Quine – Mc-Clusky minimization technique.
 $y = f(a, b, c, d) = \sum m(0, 2, 8, 10)$. (08 Marks)
 - Using the Quine – McCluskey method obtain all the prime implicants for the following Boolean function : $f(a, b, c, d) = \pi M(0, 2, 3, 4, 5, 12, 13) + dc(8, 10)$. (12 Marks)

Module-2

- With the aid of general structure, clearly distinguish between a decoder and encoder. (06 Marks)
 - Implement the following Boolean function using 4 : 1 multiplexer.
 $F(A, B, C) = \sum m(1, 3, 4, 6)$. (06 Marks)
 - Implement full subtractor using a decoder and two NAND gates and write its truth table. (08 Marks)

OR

- What is carry look ahead adder? Explain general organization of it. (06 Marks)
 - Write a truth table for two bit magnitude comparator. Write the Karnaugh map for each output of two bit magnitude comparator and the resulting equation. (14 Marks)

Module-3

- What is a Flip-Flop? Discuss the working principle of SR Flip-Flop with its truth table. Also highlight the role of SR Flip-Flop in switch de-bouncer circuit. (12 Marks)
 - Explain the operation of master slave JK Flip-Flop along with its circuit diagram. (08 Marks)

OR.

- Draw and explain the working of Positive and Negative edge triggered D flip-flop. (12 Marks)
 - Derive the characteristic equations for D, JK, T and SR Flip-Flops. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. Explain with suitable logic and timing diagram :
 i) Serial-in serial out shift register
 ii) Parallel-in parallel out shift register. (10 Marks)
- b. Compare Registers and Counters. Explain the working of 4-bit asynchronous counter configured using JK flip-flops. (10 Marks)

OR

- 8 a. Describe the block diagram of a MOD-7 Johnson counter and explain its operation. Give the count sequence table and the decoding logic used to identify the various states. (10 Marks)
- b. Design a MOD-5 synchronous binary counter using clocked JK Flip-Flops. (10 Marks)

Module-5

- 9 a. With a suitable example, explain Mealy and Moore model in a sequential circuit analysis. (08 Marks)
- b. A sequential circuit has one input and one output. The state diagram is as shown in Fig.Q9(b). Design a sequential circuit with 'T' flip-flop.

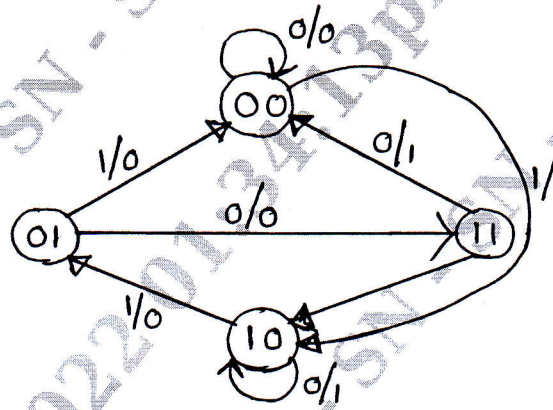


Fig.Q9(b)

(12 Marks)

OR

- 10 a. With a basic structure, explain clearly Programmable Read Only Memories (PROMS) and EPROM. (13 Marks)
- b. Write short notes on :
 i) Read only and Read/Write memories
 ii) Flash memory. (07 Marks)
